

CLAIMS

We claim:

1 1. A CIS scanning circuit comprising:
2 an inverter,
3 at least one photodiode detector serving as a scanning light sensing element,
4 an integration capacitor,
5 an AC coupling mechanism, and
6 video output means comprising at least one output source follower circuit; wherein
7 said inverter is a low-power, high-gain, single-stage inverter that serves as an
8 integration amplifier to clamp said light sensing element at a fixed bias voltage,
9 said integration capacitor has a capacitance value that is much smaller than an
10 effective capacitance of said photodiode detector, said integration capacitor being used
11 to provide a pixel gain, and
12 said AC coupling mechanism stores and cancels reset noise of said integration
13 capacitor, thereby allowing the implementation of a high sensitivity sensor with minimum
14 noise.

1 2. The CIS scanning circuit of claim 1 wherein:
2 said capacitance value of said integration capacitor is at least ten times smaller
3 than said effective capacitance of said photodiode detector.

1 3. The CIS scanning circuit of claim 1 wherein:

2 said circuit further comprises a cross-bar output structure to cancel an offset
3 voltage of each pixel introduced by a threshold variation of a pair of said output source
4 follower circuits.

1 4. The CIS scanning circuit of claim 1 wherein:

2 said photodiode detector is an n-p junction photodiode.

1 5. The CIS scanning circuit of claim 1 wherein:

2 said photodiode detector is an p-n junction photodiode.

1 6. The CIS scanning circuit of claim 1 wherein:

2 said inverter comprises at least two transistors and at least one bias voltage, one
3 of said transistors functions as a current source, and remaining ones of said transistors
4 are cascode transistors to increase gain and to isolate input and output nodes.

1 7. The CIS scanning circuit of claim 1 wherein:

2 a loading capacitor is used to reduce a frequency bandwidth of said inverter to
3 reduce a thermal noise level.

1 8. The CIS scanning circuit of claim 1 wherein:

2 said video output means comprises a cross-bar circuit including at least three
3 transistors to reset hold capacitors of said scanning circuit and to eliminate a dark offset

4 of each pixel.

1 9. The CIS scanning circuit of claim 1 wherein:

2 each pixel circuit of said scanning circuit receives input from two detectors,
3 thereby providing a lowered resolution array with higher sensitivity and lower scanning
4 time.

1 10. The CIS scanning circuit of claim 1 wherein:

2 said scanning light sensing element is an interdigitated array structure comprising
3 at least two linear arrays, said linear arrays being offset by one half pixel in an array
4 direction and one line distance in a scanning direction, each said linear array having one
5 half a desired resolution, said linear arrays being paired to achieve said desired
6 resolution, thereby providing higher sensitivity and lower cost.

1 11. The CIS scanning circuit of claim 10 wherein:

2 said linear arrays share output processing circuits, including a digital scanning
3 register, IS and IR current sources, OS and OR common video lines, and follow-on
4 differential amplifier stages, thereby providing smaller sensor chip size, lower power
5 dissipation, and higher scanning speed.

1 12. The CIS scanning circuit of claim 10 wherein:

2 each pixel circuit of said scanning circuit receives input from at least two

3 detectors, thereby providing a lowered resolution array with higher sensitivity and lower
4 scanning time.

1 13. The CIS scanning circuit of claim 10 wherein:

2 said scanning light sensing element comprises at least two linear arrays, each of
3 said linear arrays being selectively disabled to provide multiple resolution settings for
4 said scanning circuit.

1 14. A CIS scanning circuit comprising:

2 an inverter,

3 at least one photodiode detector serving as a scanning light sensing element,

4 an integration capacitor,

5 an AC coupling mechanism, and

6 video output means comprising at least one output source follower circuit; wherein

7 said scanning light sensing element is an interdigitated array structure comprising
8 at least two linear arrays, said linear arrays being offset by one half pixel in an array
9 direction and one line distance in a scanning direction, each said linear array having one
10 half a desired resolution, said linear arrays being paired to achieve said desired
11 resolution, thereby providing higher sensitivity and lower cost.

1 15. The CIS scanning circuit of claim 14 wherein:

2 said linear arrays share output processing circuits, including a digital scanning

3 register, IS and IR current sources, OS and OR common video lines, and follow-on
4 differential amplifier stages, thereby providing smaller sensor chip size, lower power
5 dissipation, and higher scanning speed.

1 16. The CIS scanning circuit of claim 14 wherein:

2 each pixel circuit of said scanning circuit receives input from at least two
3 detectors, thereby providing a lowered resolution array with higher sensitivity and lower
4 scanning time.

1 17. The CIS scanning circuit of claim 14 wherein:

2 said scanning light sensing element comprises at least two linear arrays, each of
3 said linear arrays being selectively disabled to provide multiple resolution settings for
4 said scanning circuit.

1 18. The CIS scanning circuit of claim 14 wherein:

2 said inverter is a low-power, high-gain, single-stage inverter that serves as an
3 integration amplifier to clamp said light sensing element at a fixed bias voltage,

4 said integration capacitor has a capacitance value that is much smaller than an
5 effective capacitance of said photodiode detector, said integration capacitor being used
6 to provide a pixel gain, and

7 said AC coupling mechanism stores and cancels reset noise of said integration
8 capacitor, thereby allowing the implementation of a high sensitivity sensor with minimum

9 noise.

1 19. The CIS scanning circuit of claim 14 wherein:

2 said capacitance value of said integration capacitor is at least ten times smaller
3 than said effective capacitance of said photodiode detector.

1 20. The CIS scanning circuit of claim 14 wherein:

2 said circuit further comprises a cross-bar output structure to cancel an offset
3 voltage of each pixel introduced by a threshold variation of a pair of said output source
4 follower circuits.

1 21. The CIS scanning circuit of claim 14 wherein:

2 said photodiode detector is an n-p junction photodiode.

1 22. The CIS scanning circuit of claim 14 wherein:

2 said photodiode detector is an p-n junction photodiode.

1 23. The CIS scanning circuit of claim 14 wherein:

2 said inverter comprises at least two transistors and at least one bias voltage, one
3 of said transistors functions as a current source, and remaining ones of said transistors
4 are cascode transistors to increase gain and to isolate input and output nodes.

1 24. The CIS scanning circuit of claim 14 wherein:

2 a loading capacitor is used to reduce a frequency bandwidth of said inverter to
3 reduce a thermal noise level.

1 25. The CIS scanning circuit of claim 14 wherein:

2 said video output means comprises a cross-bar circuit including at least three
3 transistors to reset hold capacitors of said scanning circuit and to eliminate a dark offset
4 of each pixel.

1 26. A CIS scanning circuit sensing element comprising:

2 an interdigitated array structure comprising at least two linear arrays, said linear
3 arrays being offset by one half pixel in an array direction and one line distance in a
4 scanning direction, each said linear array having one half a desired resolution, said linear
5 arrays being paired to achieve said desired resolution, thereby providing higher
6 sensitivity and lower cost.

1 27. The CIS scanning circuit sensing element of claim 26 wherein:

2 said linear arrays share output processing circuits, including a digital scanning
3 register, IS and IR current sources, OS and OR common video lines, and follow-on
4 differential amplifier stages, thereby providing smaller sensor chip size, lower power
5 dissipation, and higher scanning speed.

1 28. The CIS scanning circuit sensing element of claim 26 wherein:
2 each pixel circuit of said scanning circuit receives input from at least two
3 detectors, thereby providing a lowered resolution array with higher sensitivity and lower
4 scanning time.

1 29. The CIS scanning circuit sensing element of claim 26 wherein:
2 said scanning light sensing element comprises at least two linear arrays, each of
3 said linear arrays being selectively disabled to provide multiple resolution settings for
4 said scanning circuit.